AMENDMENTS TO THE CLAIMS:

A listing of the status of all claims 1-22 in the present patent application is provided below which will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) A process wherein at least two processed semiconductor wafers having electrically active structures thereon[[,]] that are located in a ~~middle position~~ central area of a stack of wafers, and wherein in an operation of a mechanical connecting, electrically insulating connections and electrically conductive connections are produced between said at least two processed semiconductor wafers each one thereof having a wafer surface to be connected, said process comprising:

providing an electrically non-conducting glass paste ~~comprising glass particles and a binder~~ and an electrically conducting glass paste ~~comprising glass particles and a binder~~;

applying patterned layers of the electrically non-conducting glass paste and the electrically conducting glass paste on said wafer ~~sides~~ surfaces;

thereafter conditioning and pre-melting the electrically non-conducting glass paste and the electrically conducting glass pastes;

thereafter providing geometrical alignment of the at least two processed semiconductor wafers to be connected; and

thereafter ~~joining~~ bonding the at least two processed semiconductor wafers at a first processing temperature of the electrically non-conducting glass paste and at a second processing temperature of the electrically conducting glass pastes using a mechanical pressure.

2. (Previously Presented) The process according to claim 1, wherein the electrically non-conducting glass paste and the electrically conducting glass paste are applied by a screen printing process.

3. (Previously Presented) The process according to claim 1, wherein the electrically non-conducting glass paste and the electrically conducting glass paste have different conditioning conditions and premelting conditions and, therefore, the conditioning and the premelting are implemented successively, each in a separate conditioning and premelting process.

4. (Previously Presented) The process according to claim 1, wherein the first processing temperature of the electrically non-conducting glass paste and the second processing temperature of the electrically conducting glass paste are the same processing temperature.

5. (Previously Presented) The process according to claim 1, wherein the first processing temperature of the electrically non-conductive glass paste and the second processing temperature of the electrically conducting glass paste are different processing temperatures and wherein the first processing temperature and the second processing temperature are successively passed in the process of joining the at least two processed semiconductor wafers.

6. (Previously Presented) The process according to claim 1, wherein at least one of the at least two processed semiconductor wafers has an electrical connection in an area that does not contain electronic structures.

7. (Previously Presented) The process according to claim 1, wherein the at least two processed semiconductor wafers are electrically connected at specific electric circuit points in areas containing electronic structures.

8. (Previously Presented) The process according to claim 1, wherein the joining of the at least two processed semiconductor wafers further comprises the first processing temperature and the second processing temperature being about 450°C.

9. (Previously Presented) The process according to claim 1, wherein one of the at least two processed semiconductor wafers is a SOI wafer comprising an active semiconductor layer and a buried oxide layer on a substrate and wherein an electrical connection to the substrate of the SOI wafer is implemented through previously produced openings in the buried oxide layer and in ~~an~~ the active semiconductor layer.

10. (Cancelled)

11. (Withdrawn) A process for bonding processed semiconductor wafers as system wafer supporting micro-electromechanical or electronic structures with a cover wafer also supporting electronic structures, wherein in an operation of bonding, electrically insulating connections and electrically conductive connections are produced between the semiconductor wafers, said process comprising:

applying a first electrically non-conducting, structured layer and a second electrically conducting structured layer, each one with a glass paste on at least one face of the wafers to be bonded together,

conditioning of the glass pastes;

geometrical alignment of the wafers to be bonded;

joining the wafers together at a processing temperature of the glass pastes using a mechanical pressure.

12. (Withdrawn) The process according to claim 11, wherein the glass pastes are applied with a screen printing process.

13. (Withdrawn) The process according to claim 11, wherein the non-conducting glass paste is low-melting and the electrically conducting glass paste has a different premelting condition and premelting of each of the pastes is implemented successively in a separate process.

14. (Withdrawn) The process according to claim 11, wherein the non-conducting glass paste is low-melting and the electrically conducting glass paste has a substantially same processing temperature.

15. (Withdrawn) The process according to claim 11, wherein the non-conducting glass paste is low-melting and the electrically conducting glass paste has a different processing temperatures.

16. (Withdrawn) The process according to claim 11, wherein at least one of the wafers is electrically connected in a wafer area not structured electronically.

17. (Withdrawn) The process according to claim 11, wherein at least one of the wafers is electrically connected at a specific electric circuit point located in an electronically structured area of the wafer.

18. (Withdrawn) The process according to claim 11, wherein a glass paste connection formation takes place at a temperature of less than 450°C.

19. (Withdrawn) The process according to claim 11, wherein the electric connection of a substrate of an SOI wafer is implemented through at least one previously produced opening in a buried oxide layer of said SOI wafer and in an active silicon layer, of said SOI wafer whereby at least one wall area of the at least one opening in the active silicon layer being provided with an insulating layer prior to the electric connection with the conducting glass paste.

20. (Cancelled)

21. (Previously Presented) The process according to claim 1, wherein the applying of the patterned layers comprises applying a first patterned layer of the electrically non-conducting glass paste to the wafer surface side of a first one of the at least two processed semiconductor wafers and applying a second patterned layer of the electrically conducting glass paste on the wafer surface side of a second of of the at least two processed semiconductor wafers.

22. (Currently Amended) A process wherein at least two processed semiconductor wafers having electrically active structures thereon[[,]] that are located in a ~~middle position~~ central area of a stack of wafers, and wherein in an operation of a mechanical connecting, electrically

insulating connections and electrically conductive connections are produced between said at least two processed semiconductor wafers, each one thereof having a wafer surface to be connected, said process comprising:

providing an electrically non-conducting glass paste ~~comprising glass particles and a binder~~ and an electrically conducting glass paste ~~comprising glass particles and a binder~~;

applying a patterned layer of electrically non-conducting glass paste on said wafer ~~sides~~ surfaces;

thereafter conditioning and pre-melting the electrically non-conducting glass paste on said wafer ~~sides~~ surfaces;

applying a patterned layer of electrically conducting glass paste on said wafer ~~sides~~ surfaces;

thereafter conditioning and pre-melting the electrically conducting glass paste on said wafer ~~sides~~ surfaces;

thereafter providing geometrical alignment of the at least two processed semiconductor wafers to be connected; and

thereafter ~~joining~~ bonding the at least two processed semiconductor wafers at a first processing temperature of the electrically non-conducting glass paste and at a second processing temperature of the electrically conducting glass pastes using a mechanical pressure.